SECTION 13580
MICROPROCESSORS

PART 1 – GENERAL

1.01 DESCRIPTION

A. The contractor shall furnish a MicroLok II Vital Microprocessor Based Interlocking System (VMIS) and Non-Vital Based Interlocking Systems (NVMIS) for each new interlocking in accordance with the requirements contained herein.

B. The contractor shall furnish a MicroLok II Vital Microprocessor Based Interlocking System (VMIS) for each traffic light control location which requires new TLC control in accordance with the requirements contained herein.

1.02 QUALITY ASSURANCE

A. The VMIS must conform to the standards of AREMA Communication and Signal Division, Part 2.2.12, National Electrical Manufacturers Association (NEMA), the Institute of Electrical, Electronic Engineers (IEEE) and the Federal Railroad Administration (FRA).

B. The contractor shall designate vital hardware as hardware which under failure can adversely affect the safety of train or vehicular movements. Further, if the safe implementation of a vital function is dependent in whole or in part on the absence of failures in the hardware circuit or device, then that hardware is vital. Vital hardware is hardware whose failure modes and characteristics can be accurately identified, predicted and exhaustively tested. The occurrences of failure modes that could have unsafe consequences are eliminated, prevented, or otherwise accounted for by design.

C. Provide materials and equipment designed to operate in accordance with all applicable AREMA and local code requirements for Vital and Non-Vital Electronic Hardware being installed under this Contract. Provide all systems and equipment to be in compliance with a Contractor standard quality assurance program.

D. Provide electrical and electronic components rated to operate at power, voltage, current, and temperature levels exceeding by 20 percent those that the components will be subject to in service, unless otherwise specified herein.

1.03 SUBMITTALS

A. Unless otherwise waived by the SEPTA Project Manager, submit complete performance data information and a sample of each type of new component or product as an equivalent to those herein specified. [CDRL 13580-001] Obtain the
SEPTA Project Manager’s written approval for any such equivalent type component or product before proceeding with manufacturer or procurement.

B. CDRLs

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1.04 DELIVERY AND HANDLING

A. The Contractor shall be responsible for any damages in the shipment and handling of all NVMIS and NVMIS equipment and appurtenances under this Contract.

B. All PCB cards shall be shipped in Static Shielding Bags.

C. All VMIS and NVMIS equipment cabling shall be secured from coming loose in transit.

PART 2– PRODUCTS

2.01 GENERAL

A. The Contractor shall provide MicroLok II Vital Microprocessor Interlocking System’s to meet all requirements of these Technical Specifications and Contract Drawings.

B. All NV/VMIS shall consist of, but not be limited to, chassis, racks, CPU circuit cards, I/O circuit cards, power supplies, cabling, terminations, serial communications links, Ethernet network links, executive software, application software, diagnostic software, remote monitoring software and all other subsystems and components related to the system.

C. The NV/VMIS shall be designed to operate in a hot standby redundant configuration with an automatic transfer to the redundant system in the event of a failure to the primary unit. The automatic transfer shall take effect immediately upon detection of the loss of the primary processor without interfering with established routes or operations.
D. A manual transfer of the processors shall be supplied to allow a technician to switch from the primary to the secondary or vice versa to allow for testing or otherwise.

E. The Contractor shall be responsible for integrating all components of the NV/VMIS. The Contractor shall provide product from manufacturers that provide a complete set of required circuit cards. Mixing and matching multiple vendors is not permitted.

F. The microprocessor based equipment shall be applied in a fault tolerant configuration as defined within these Technical Specification and Contract Drawings. This application shall apply for interlockings, TLC and other safety and service critical applications. The Contractor shall only furnish systems with a proven record of in-service applications that meet these requirements in operating environments similar to that found on the MSHL.

G. All microprocessor based equipment provided for a specific interlocking, TLC location or interface location shall be housed within enclosures installed at those locations where the equipment is intended to monitor or control. No distribution of the microprocessor based equipment is permitted across multiple enclosures for a single location.

H. All V/NVMIS equipment shall be the Microlok II unit as manufactured by Ansaldo STS and shall be outfitted as follows:
   1. All vital input and output Printed Circuit Boards (PCB’s) shall be the 12VDC sourcing type.
   2. All non-vital input and output PCB’s shall be the 12VDC sourcing type.
   3. All vital PCB’s shall provide for 16 inputs or outputs or any combination of inputs and outputs.
   4. All non-vital PCB’s shall provide for 32 inputs or outputs or any combination of inputs and outputs.
   5. The unit shall be mountable in a standard 19 inch rack.

I. Each V/NVMIS unit shall be provided with, as a minimum:
   1. CPU, communications, vital kill relay drive and power supply PCB’s and cables,
   2. Two (2) Standard Vital Input PCB’s and cables,
   3. Two (2) Standard Vital Output PCB’s and cables,
   4. Two (2) Non-Vital PCB’s and cables,

J. Event recorder inputs for each event recorder used on the project shall be submitted to the SEPTA Project Manager for approval prior to completing each location design.

K. Microprocessor Systems shall meet all performance requirements as defined within these Technical Specifications.
L. The communications protocol and system configuration shall allow any microprocessor connected to the network to communicate vitally with any other microprocessor that is also connected to the same network.

M. A CBTC interface to the interlocking shall provide for traffic direction and block occupancy logic and any other signal functions required by the Contractor’s final approved design to be provided. CBTC shall indicate block occupancy and direction of travel to adjacent interlockings. It shall be possible to determine from the Local Control Panels that a block is occupied and the direction of travel.

N. The Contractor shall provide a system that is immune to the effects of any electromagnetic or electrical interference generated from within or outside the instrument housings.

O. All input and output circuit cards or other components within the microprocessor system shall be so designed in a manner that will not generate any nuisance system alarms or system resets when the inputs or outputs of the circuit cards or wiring to and from the card are exposed to the normal collapsing fields developed during the operation of vital relays, non-vital relays or signal line circuits.

P. The Contractor shall provide a vital microprocessor-based interlocking control system that does not generate, or is susceptible to the generation of any electromagnetic or electrical interference generated from within or outside the instrument housings.

Q. Protection devices external to the circuit card or to external wiring or relays shall be limited to surge arresting devices for protection when components are exposed to conducted over-voltage or induced over-current field gradients. The location of signal equipment and normal wiring practices shall be permitted, without any restrictions, for future additions or modification of the system after delivery and commissioning.

R. The Contractor shall develop methods to test and verify that the application or designs proposed meet these requirements. The Contractor shall submit a test plan to be performed during the factory test to validate the design, placement of relays and wiring. [CDRL 13580-002]

2.02 MICROPROCESSOR HARDWARE AND SOFTWARE

A. Microprocessor Application Logic is software whose execution is required for the implementation of a function. As such, microprocessor’s software is a combination of system executive and application logic required for the implementation of a functions. Vital software shall be designed such that its execution cannot result in an output that is in conflict with established fail safe rules.

B. All software used by the VMIS and NVMIS shall be in the form of Boolean Statements / Logical equations
2.03 FUNCTIONAL DESIGN REQUIREMENTS

A. The vital microprocessor-based system shall consist of microprocessors, which use a closed loop feedback and independent system diagnostics to maintain vital integrity. System outputs shall be positively monitored with independent current/voltage sensors and compared to the requested value. A vital “kill” circuit shall be used to de-energize all outputs and shut down the system when the outputs fail to correspond to the required state. The central processing unit shall be continually tested to ensure all instructions are being executed properly and that processor integrity is being maintained.

B. Transmission of false information from a non-vital to a vital subsystem shall in no way affect the safety of the system. Non-vital visual indications, such as LED lamps, shall demonstrate that the system is functioning properly; similarly, failure and diagnostic indications shall be provided. Indications shall isolate a failure to a particular function, or to the interface between two functions.

C. Inputs shall be buffered and shall be immune to contact bouncing and shall be electrically and physically isolated from one another. Processor communication with each input shall vitally assure that the proper input and input state (on or off) is read. A non-vital visual indication, such as an LED lamp, shall be provided for each input on the input boards to indicate when the input is activated.

D. Outputs shall be electrically and physically isolated from one another. A vital means of verifying the proper state of the output shall be provided. Processor communication with each output shall vitally assure that the proper output is in the proper state (on or off). A non-vital visual indication, such as an LED lamp, shall be provided on the output boards for each output to indicate when the output is activated.

E. The user interface for programming site specific microprocessor application logic shall be easy to use and shall only require knowledge of interlocking and crossing system design to configure or reconfigure a control system.

2.04 VITAL SOFTWARE

A. Only through special application of hardware and software in which the failure modes and effects can be revealed and proven to meet defined values of probability of occurrence and outcome can a microprocessor be classified as a vital device.

B. The site-specific, vital logic shall define the operation of the microprocessor system, and shall include, but not be limited to the following control logic:

1. Route Check
2. Signal Control
3. Clear Block Control
4. Signal Lighting
5. Signal Indication
6. Approach and Time Locking
7. Route Locking
8. Detector Locking
9. Indication Locking
10. Switch Locking
11. Switch Control
12. Switch Indication
13. Switch Correspondence
14. Switch Blocking
15. Track Blocking
16. Loss of Shunt Protection
17. Crossing Control
18. Crossing Release
19. Trolley Direction
20. Traffic Locking
21. Generation of speed commands and or restrictions

C. Vital timing functions for locking and crossing control requirements shall be field settable and adjustable, without the need to change the site specific application logic.

D. System software of two types shall be functionally dependent upon each other to perform all vital and non-vital microprocessor logic.

E. Executive system software shall be provided by the Contractor that performs all functions necessary to provide for the proper and safe operation of the microprocessor unit as specified.

F. Application software shall be user-defined for site specific application and interfacing with all necessary subsystems.

G. Nomenclature shall be consistent with standard North American railroad nomenclature as described by APTA, AREMA and SEPTA practices, and one type of nomenclature shall be consistently used for each application program used on the project. Nomenclature shall distinguish I/O from internal variables. Inputs shall be distinguished from outputs and the I/O nomenclature shall reference the logical unit on the other side of the interface, i.e., the input or output device. Variables of vital functions shall be distinguished from those of non-vital functions. New or special function designators shall be as simple as possible, but not conflict or lead to confusion with established function designations.
H. The source application for the system shall be provided as a readable hardcopy and in a word processor text file. [CDRL 13580-003] The format shall be submitted to the Project Manager in Microsoft Word.

I. Changes in the application logic shall not require recompilation, verification and/or validation of the executive software.

J. The logic shall be as simple as possible, expressed in a high-level, structured and easily understood Boolean form. Application logic programming shall be in accordance with SEPTA's standards and practices. Organization and adequate commenting are an inherent quality of the safety of the logic, i.e., the readability/understandability of the logic and logic organization are integral to the long-term safe operation and maintenance of the system. Therefore, comments may be applied liberally throughout the software.

K. General organization of the application programming logic, in the order appearing in the program listing shall be:

1. Program name, version level, programmer, checker, etc.
2. Machine specific requirements in the programming (e.g., compiler switches)
3. General remarks, comments, special features, etc.
4. Hardwire I/O bit definition
5. Serial I/O bit definition
6. Internal Variables bit definition
7. Timers
8. Logged Bits
9. Configuration (Application Parameters)
10. Logical Assign Statements
11. Look Up Tables (if required)
12. Numeric Blocks (if required)

L. Loss-Of-Shunt (LOS) protection shall be provided by five second (5s) timing (i.e., delayed application of an input and/or internal variable). The Five Second LOS shall be implemented at the track detector level. This timing shall be performed in the processor which is processing the inputs and not by a processor removed from the input to be timed by intermediate processing units or stages. Five second loss-of-shunt protection for route locking shall NOT be performed at the switch locking or route locking level.

2.05 MICROPROCESSOR HARDWARE

A. As identified in the General Statement of Work, there are 27 (twenty-seven) 28 (twenty-eight) existing highway crossings equipped with Ansaldo STS MicroLok
II® vital processors for traffic light control. The contractor will incorporate the existing MicroLok II processors into the overall CBTC system architecture.

B. Spare input and output board slots are required. Vital microprocessor motherboards shall allow the addition of inputs and outputs by the purchase of input/output boards and simple installation by SEPTA. A minimum of 25% of all of the inputs and 25% of all of the outputs used at an interlocking shall be provided as spare at each interlocking.

C. A complete set of vital and non-vital microprocessor printed circuit boards shall be provided, including processor board, input boards, output boards, power supply boards, etc. for each new processor supplied on the project.

D. SEPTA Project Manager approved labels shall be provided by each input and output indication which clearly denote the respective function of each, for the ease of maintenance and troubleshooting.

E. Power for the output circuits shall be supplied through a vital cut-off circuit. This circuit shall be driven by a vital clock signal generated by the processor checks and diagnostics. The vital clock signal shall pass through filters tuned to prevent a false signal from energizing the relay. The signal frequency shall be chosen such that it could not be generated by any other device in the equipment housing: for example, 60 Hz power supplies or battery chargers, audio frequency overlay equipment, or harmonics of these devices. The vital cut-off circuit shall remove the vital clock signal and de-energize the vital cut-off relay.

F. The vital processors shall control several output devices, which shall be energized with 12VDC, such as vital signal control relays. Output boards shall withstand without damage, the shorting of the output to ground or the opposite DC polarity.

G. All power for the vital microprocessor interlocking shall be properly isolated from the effects of electromagnetic interference, lightning, noise, current surges, and grounds. Surge suppressor units to further enhance this isolation are required by this Contract and shall be provided by the Contractor.

H. A SEPTA Project Manager approved vital means of indexing PCBs, either mechanically or in software, shall be implemented to ensure that only the proper PCBs are inserted in card slots.

I. All components of the system shall operate at temperatures of minus 40 degrees Centigrade to plus 70 degrees Centigrade, and humidity levels of 0 - 95% non-condensing without any external environmental controls.

J. All 'dirty' wiring (wiring not protected or isolated from the effects of electromagnetic interference, lightning, noise, current surges and grounds) shall be kept clear of the vital microprocessor wiring as far as is practical and where that is not possible, the wiring methods shall utilize other means to protect against induced interference.
K. All major assemblies, subassemblies, circuit cards and devices shall be permanently marked with the manufacturer's part identification number.

L. All ICs, PCBs, components, etc., which are subject to revision (such as PROMs) and/or are removable from assemblies, should have the revision level identified on the component.

M. The Contractor shall be responsible and verify that the equipment functions in a manner intended in the environment in which it is to be installed and operated.

N. Microlok’s are provided with internal event recorder. The contractor shall submit to the Project Manager a list of bits to be recorded by the event recorder. [CDRL 13580-004]

2.06 NON-VITAL SOFTWARE

A. The non-vital code system shall include, but not be limited to the following controls, which are listed below:

1. Route Setting
2. Signal Request/ Cancel
3. Switch and Signal Operation
4. Route Cancellation
5. Switch Blocking
6. Track Blocking
7. Snowmelter Control
8. Clear Block Signal Control

B. The non-vital code system shall include indication data to enable display update at the Operations Control Center. The indications shall include, but not be limited to the following indications, which are listed below:

1. Signal Status
2. Switch Position
3. Switch Locking
4. Route Setting
5. Traffic Direction
6. Snowmelter Status
7. Track Occupancy - Block Status
8. Control from Auto or Manual
9. Fleeting Status
10. Clear Block Signal Status
11. Intrusion
13. Fire Alarm
14. AC and DC Power Off
15. Grounds
16. Surge Faults
17. Fire Suppression System Fault Alarms
18. All other alarms and indications as may be required and that are specified in other Technical Specification sections.

C. Indications to the Operations Control Center shall be positive true unless otherwise approved by the SEPTA Project Manager.

2.07 SYSTEM DIAGNOSTICS

A. The Contractor shall provide a Remote Diagnostic System (RDS) as part of this contract. Access to all microprocessor systems is required through this system. All aspects of the system to be provided shall be submitted for review and approval by the SEPTA Project Manager. [CDRL 13580-005]

B. The Contractor shall provide three (3) workstations to access the RDS. These workstations will be located at three discrete locations within the SEPTA operating territory.

C. The system provided shall permit SEPTA Maintenance and Technical personnel to remotely access all diagnostic aspects of the field systems normally available locally through a laptop or vendor specific interface. Whatever can be accessed, monitored, viewed, alarmed, controlled or changed locally shall be likewise available remotely through the RDS. This will include the state of all software variables, I/O status, Timer status, communications status as well as all failure bits, errors and alarms.

D. The RDS shall provide security levels to restrict unauthorized user access to the system and to permit various level of authorization for different functions provided.

E. When alarm conditions are received, further diagnostic functions shall be provided to analysis the exact problem.

F. This system shall allow access to the processor health, control and indication status and to invoke diagnostic and maintenance functions, including remote trouble shooting to the circuit board level.

PART 3– EXECUTION

This Part not used in this Section.

END OF SECTION 13580